In the claims:

All of the claims standing for examination are presented below with appropriate status indication.

1. (Currently amended) A ~~secure memory device for use with and contained within a~~ dual-purpose smart card ~~with a modem interface~~ comprising ~~circuitry of~~:

~~a rewritable memory~~ a standard ISO 7816 eight-pad array including a reset (Rst) pad and an I/O pad;

~~a processing unit or a microprocessor;~~

~~an on-chip oscillator, circuitry of which is contained in the secure memory device;~~

~~an ISO 7816 interface~~ digital storage media and first electronic circuitry compliant with ISO 7816 standards and connected to the pad interface, enabling the card apparatus to be used as a conventional smart card;

an oscillator connected through a one-wire modem to the I/O pad, enabled to provide a modulated voltage on the I/O pad; and

control circuitry enabled to control functions of the first electronic circuitry and the one-wire modem;

~~a one-wire modem interface;~~

~~characterized in that both communication interfaces are bidirectional and share a single I/0 terminal providing a single connection port on the secure memory device for both of the communication interfaces~~ wherein, with the Rst pad high the one-wire modem is inactive and the first electronic circuitry is active enabling the smart card to function as a standard smart card through the ISO 7816 interface with a conventional card reader, and with the Rst pad low, the first electronic circuitry is disabled, and the one-wire modem is enabled, providing a modulated voltage signal on the I/O pad.

2-28. (Cancelled)

Remarks

The present Response is to the Office Action mailed 10/28/2008. Claims 1-11, 13-25, 27 and 28 are presented for examination.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/6/2008 has been entered.

Applicant's response: Acknowledged

Response to Arguments

2. Applicant's arguments filed 106/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. Prior art of record does not teach an "on-chip" oscillator.

b. Prior art of record does not teach "a single connection port"

3. In response to argument 'a', examiner notes that the cited portions of prior art, Atsmon, are directed to a processor (PIC 16F84), and therefore on-chip clearly means on the processor chip. However, the memory card itself contains a layer of silicon on which the processor and other circuits are printed. Therefore, while the oscillator is not on the processor, it is still on the silicon portion of the memory card, which is interpreted as on-chip. Likewise, there is no mention that applicant's oscillator is on the processor portion of the memory card, but merely that the oscillator is on-chip, or "circuitry of which is contained in the secure memory device" as claimed.

4. Examiner further notes that the actual uses cited by the applicant of the modem interface (FSK and PSK) are not cited in the claims, and therefore cannot be relied upon to exclude uses of the oscillator. It is reminded that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993).

5. In response to argument 'b', examiner notes that the single connection port in the prior art is the port which the multiple interfaces use to communicate with the processor. It is clear that all the interfaces (ISO, USB, wireless) all are converged into a single interface for the processor as shown in the rejection. While prior art might not explicitly state this, it is implied in the drawing and the cited portions of the prior art. If all three interfaces did not share the single connection port into the processor, then why does the prior art does show three separate ports into the processor? Furthermore, why would it be necessary to convert these three types of data?

Examiner further notes that the claim does not specify the communication counterparts of the connection port. In other words, the claim does not specify that the single connection port communicates with two different interfaces of the host, and therefore does not preclude that the single connection port is used to communicate data between the internal processor and three cited interfaces.

6. Having responded to each of applicant's arguments, examiner notes that prior art of record still provides a valid ground of rejection, as attached below.

Applicant's response: The claims are significantly narrowed in the present response, and the specific references to limitations in the rejections no longer apply. Still the applicant wishes to point out that the claimed "single connection port" is in reality a single pad in the ISO pad array, and this has been clarified in the new claim language. Whether the single connection port communicates with two different interfaces in the host is immaterial, as the host is not claimed. The purpose of the one-wire modem and the ISO I/O port sharing the same pad is simple that the card can be used as either a conventional smart card, or a special card communicating a security signal to a host.

Claim Rejections - 35 USC § 103

8. Claims 1, 2, 15,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsmon et al (US Patent #6,607,136) in view of Leydier et al (PG Pub #US 2003/0046554 A1)

9. Regarding claim 15, Atsmon discloses a secure memory device (system shown in figure 1) for use with and contained within a smart card with a modem interface comprising circuitry of:

A rewritable memory (memory unit 22, figure 2; column 12, lines 38-42);

A processing unit or a microprocessor (processing unit 21);

An on-chip oscillator (oscillator circuit or RC circuit; column 13, lines 4-11), circuitry of which is contained in the secure memory device; examiner notes that Atsmon teaches both circuits being external. However, both circuits are external to the processor, not to the card. This is evidenced by the fact that Atsmon teaches the type of oscillator used is limited by the size of the card. Atsmon also teaches that the oscillator would be connected to the OSC1/CLKIN pin of the processor (figure 7).
Accordingly, examiner asserts that the oscillator is on-chip (on the card).

An ISO 7816 interface (column 25, lines 12, 13);

A one-wire modem interface (transducer; column 11, lines 37 -39);

Characterized in that both communication interfaces are bidirectional (input/output unit 35, figure 3; column 11, lines 36-40); Examiner notes that the I/O unit 35 can both receive and transmit data (therefore bi-directional).

Atsmon does not disclose explicitly that both communication interfaces share the same I/O terminal. However, Leydier discloses a smartcard (figure 13) such that communication interfaces (ISO, USB, Wireless ports) share a single I/O terminal (communication interface 190, paragraph 59) providing a single connection port on the secure memory device for both of the communication devices (figure 13, connection port to processor 169). Teachings of Atsmon and Leydier are from the same field of smartcards, and specifically of multiple communication interface smartcards.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Atsmon and Leydier by using a common I/O terminal in the smartcard system of Atsmon for the benefit of converting data between different protocols (paragraph 59).

10. Regarding claim 2, Atsmon further discloses a secure memory of device as in claim 1, exchanging data with a host in the form of a modulated signal by means of a card reader reading the smart card (air, column 15, line 7), the smart card characterized by possessing all processing means required for exchanging data with the card reader (examiner notes that both Atsmon and Leydier teaches that the medium of transmission could be air, i.e. wireless transmission of acoustic signals).

11. Claims 3-11, 13, 14, 17-25, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsmon and Leydier further in view of Saitoh (US Patent # 5,929,414).

12. Regarding claim 3, Atsmon and Leydier combined discloses claim 2, but does not disclose explicitly when a reset input that controls activation of ISO interface and modem interface. However, Saitoh discloses a memory device (figure 1) wherein an ISO interface (contact 55) is active when a reset input is high, and a modem interface (modem 57) is active when the reset input is low (column 5, lines 22-43; lines 59-65). Examiner notes that Saitoh discloses the modem being activated and connected to the CPU when VCC from a contact reader/writer is off. This means that reset input is also low (off) because a contact reader/writer provides a reset ON only when VCC is on.

Teachings of Atsmon, Leydier and Saitoh are from the same field of IC cards, and specifically of communication interface design of IC cards. Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to combine teachings of Atsmon, Leydier and Saitoh by using the selector circuitry and logic in the combined IC card system for the benefit of switching between contact and contact-less data transfer in one IC card (column 2, lines 35-38).

13. Regarding claim 4, Atsmon, Leydier and Saitoh combined disclose claim 3, where Saitoh further discloses transmitting a modulated answer to reset to the host when the reset intput is pulled down (column 3, lines 65-68; column 4, lines 1-2). Examiner

notes that modem (contact-less interface to reader/writer) also conforms to ISO 7816-3, and therefore must communicate with the reader/writer in the same formal. This is further evidence by Saitoh's teachings of a reader/writer that communicates with either contact or contactless IC cards (column 8, lines 29-40).

14. Regarding claim 5, Atsmon, Leydier and Saitoh combined disclose claim 4, where Saitoh further discloses transmitting the MAR only once, when the card is inserted into the card reader (column 8, lines 29-51). Examiner notes this operation is also defined by ISO standard 7816.

15. Regarding claim 6, Atsmon, Leydier and Saitoh combined disclose claim 5, where Saitoh further discloses where the MAR comprises at least three fields, a header, a card number and a random number. Examiner notes these fields are according to ISO standard 7816.

16. Regarding claim 7, Atsmon, Leydier and Saitoh combined disclose claim 6, where Saitoh further discloses computing a new random number prior to transmit the MAR. Examiner notes this again is a requirement of ISO standard 7816.

17. Regarding claim 8, Atsmon, Leydier and Saitoh combined disclose claim 3, where Atsmon further discloses transmitting data to and receiving data from a PC by means of a card reader plugged into the microphone input and the speaker output of the PC sound card (figure 1; column 31, lines 29-52).

18. Regarding claim 9, Atsmon, Leydier and Saitoh combined disclose claim 8, but does not disclose explicitly powered by voltage provided by the microphone input of the sound card. Examiner asserts that it would have been obvious for a person of ordinary skill in the art at the time of invention to provide power to the card using the a source on the host or card reader because it would eliminate need of a power source on the card, which is further evidenced by teachings of Leydier (paragraph 60).

19. Regarding claim 10, Atsmon, Leydier and Saitoh combined disclose claim 3, and Atsmon further discloses transmitting data to and receiving data from an IVR server by means of a card reader plugged into the telephone line (column 10, lines 60-65; column 20, lines 1-18).